PLEASE AMEND THE CLAIMS AS FOLLOWS, UNMARKED VERSION:

1. (AMENDED) A method of preventing copper diffusion in the fabrication of an integrated circuit by means of a composite diffusion barrier layer, and forming conducting inlaid copper, the method comprising the following steps:

(a) providing a substrate or wafer having an insulator layer deposited upon said substrate;

(b) providing a first level of conducting wiring over said insulator layer;

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(c) depositing a first and second dielectric layer over said first level of conducting wiring;

(d) patterning and etching the dielectric layers forming dual damascene trench/via openings;

(e) depositing a WN first barrier layer over said dielectric layers covering and lining said trench/via;

(f) soaking said WN first barrier layer in a reactive silane gas mixture forming a WSiN layer on the WN;

(g) depositing a W barrier layer over the WN first barrier layer and on the WSiN layer, forming over dual damascene trench/via openings, by the above process steps (a) to (g), a composite diffusion barrier layer comprised of W/WSiN/WN, with a WN first barrier layer, followed by a WSiN layer on the WN first barrier layer, and then followed by a W barrier layer on the WSiN layer;

(h) depositing by electrochemical deposition a copper seed layer over the diffusion barrier layer;

(i) depositing by electrochemical deposition a copper conducting material on the copper seed layer forming an excess of copper, and removing the excess material, thus forming conducting inlaid copper.

5. (AMENDED) The method of claim 1, wherein the W barrier layer on the WSiN layer is deposited by chemical vapor deposition (CVD) or by physical vapor deposition (PVD), sputtering, in the thickness range from about 30 to 50 Angstroms.

6. (AMENDED) The method of claim 1, wherein the trench or channel and via hole contact is lined with a diffusion barrier layer comprised of a composite diffusion barrier layer comprised of W/WSiN/WN, with a WN first barrier layer thickness from about 30 to 50 Angstroms, followed by a WSiN layer on the WN first barrier layer thickness from about 30 to 60 Angstroms, and then followed by a W barrier layer thickness from about 30 to 50 Angstroms on the WSiN layer.

9. (AMENDED) The method of claim 1, wherein the copper seed layer is deposited by physical vapor deposition sputtering, and the seed layer material is

comprised of copper metal thickness from about 1,000 to 2,200 Angstroms.

10. (AMENDED) The method of claim 1, wherein the copper conducting material on the copper seed layer for subsequent conducting interconnect lines and via contacts is comprised of the following conducting type materials: electrochemical deposition of copper, upon the copper seed layer.

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11. (AMENDED) The method of claim 1, wherein the copper conducting material on the copper seed layer is electrochemically deposited in the trench/via structures with a wide process window upon said seed layer and said barrier layer, with a fine grained <111> texture.

12. (AMENDED) The method of claim 1, wherein the excess of copper is planarized by removing excess material, the method being selected from the group comprised of: planarization by chemical mechanical polish (CMP), milling, ion milling, and/or etching, which leave the copper in trench/via openings, forming single and dual inlaid structures that include conducting interconnect lines and contact vias.

13. (AMENDED) The method of claim 1, wherein multilevel conducting inlaid copper is fabricated by repeating the process steps (c) through (i) described herein.

14. (AMENDED) A method of preventing copper diffusion in the fabrication of an integrated circuit by means of a composite diffusion barrier layer, and forming conducting damascene inlaid copper, the method comprising the following steps:

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(a) providing a substrate or wafer having an insulator layer deposited upon said substrate;

(b) providing a first level of conducting wiring over said insulator layer;

(c) depositing a first and second dielectric layer over said first level of conducting wiring;

(d) patterning and etching the dielectric layers forming dual damascene trench/via openings;

(e) depositing a WN first barrier layer over said dielectric layers covering and lining said trench/via;

(f) soaking said WN first barrier layer in a reactive silane gas mixture forming a WSiN layer on the WN;

(g) depositing a W barrier layer over said WN first barrier layer and over said WSiN layer, forming a composite barrier layer consisting of top layer to bottom layer of W/WSiN/WN diffusion barrier layer;

(h) depositing by electrochemical deposition (ECD) a copper seed layer over said diffusion barrier layer;

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(i) depositing by electrochemical deposition (ECD) copper conducting material over said copper seed layer forming an excess of copper, and removing the excess material layers to form conducting damascene inlaid copper, in the fabrication of copper interconnect wiring and contact vias.

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26. (AMENDED) The method of claim 14, wherein multilevel conducting structures are fabricated by repeating the process steps (c) through (i) described herein.